Abstract

Resolving timing violations introduced by a logic built-in self test (LBIST) sub-circuit formed within an underlying integrated circuit includes analyzing a circuit path-list corresponding to the integrated circuit for timing violations and generating a circuit timing violations analysis output; generating a first LBIST/circuit path-list based on the circuit path-list and an LBIST path-list corresponding to the LBIST sub-circuit; analyzing the first LBIST/circuit path-list for timing violations and generating an LBIST/circuit timing violations analysis output; comparing the LBIST/circuit timing violations analysis output with the circuit timing violations analysis output; generating an LBIST/circuit constraint file based on the comparison and predetermined protocols; and generating a second LBIST/circuit path-list based on the circuit path-list, the LBIST path-list and the constraints file. In this way, timing problems are quickly and efficiently resolved.